AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently Amended) Apparatus for data processing, said apparatus comprising:

(i) a shifting circuit;

(ii) an arithmetic circuit; and

(iii) an instruction decoder responsive to an instruction to control said shifting circuit and said arithmetic circuit to perform an operation using ~~upon~~ a first input data word ~~Rn~~ and a second different input data word ~~Rm~~, wherein said operation yields a result value given by:

(iv) selecting a plurality of non-adjacent multibit portions of said first input data word ~~Rm~~ to form a plurality of multibit portions each of bit length A;

(v) optionally shifting said plurality of non-adjacent multibit portions by a common shift amount to shifted bit positions;

(vi) promoting each of said plurality of non-adjacent multibit portions from said bit length of A to a bit length of B to form a plurality of promoted multibit portions, such that said promoted multibit portions may be abutted to form a promoted data word ~~P~~; and

(vii) performing a plurality of independent arithmetic operations using as input operands respective bit position portions of bit length B from both said promoted data word ~~P~~ and said second different input data word ~~Rn~~ to form a result data word ~~Rd~~.

2. (Original) Apparatus as claimed in claim 1, wherein B = 2 * A.

3. (Original) Apparatus as claimed in claim 1, wherein said plurality of multibit portions are shifted to shifted bit positions such that a lowest bit position multibit portion extends up from a zeroth order bit position.

4. (Original) Apparatus as claimed in claim 1, wherein promoting said multibit portions from a bit length of A to a bit length of B comprises one of:

(i) sign extending said multibit portions to a bit length of B; and

(ii) zero extending said multibit portions to a bit length of B.

5. (Original) Apparatus as claimed in claim 1, wherein said plurality of independent arithmetic operations are independent add operations.

6. (Currently Amended) Apparatus as claimed in claim 1, wherein said ~~data words~~ first input data word and said second different input data word each have a bit length of C and C = N * B, where N is an integer greater than 1.

7. (Currently Amended) Apparatus as claimed in claim ~~2~~ 6, wherein C = B * 2.

8. (Original) Apparatus as claimed in claim 1, wherein B = 16 and A = 8.

9. (Original) Apparatus as claimed in claim 1, wherein said common shift amount is B – A.

10. (Original) Apparatus as claimed in claim 1, wherein said instruction is a single-instruction-multiple-data instruction.

11. (Original) Apparatus as claimed in claim 1, wherein said instruction combines a data value unpack operation with an arithmetic operation.

12. (Original) Apparatus as claimed in claim 1, wherein said shifting circuit is upstream of said arithmetic circuit in a data path of said apparatus.

13. (Original) Apparatus as claimed in claim 1, wherein a promoting circuit operable to promote said multibit portions from a bit length of A to a bit length of B is disposed in parallel to a portion of said shifting circuit, said shifting circuit being operable to provide a restricted range of common shift amounts for data values passing through said shifting circuit when executing said instruction compared to a range of common shift amounts provided by said shifting circuit when executing other instructions.

14. (Currently Amended) A method of data processing, said method comprising the steps of decoding and executing an instruction on a first input data word and a second, different input data word that yields a result value given by:

(i) selecting a plurality of non-adjacent multibit portions of said first input data word ~~Rm~~ to form a plurality of multibit portions of bit length A;

(ii) optionally shifting said plurality of non-adjacent multibit portions by a common shift amount to shifted bit positions;

(iii) promoting each of said plurality of non-adjacent multibit portions from said bit length of A to a bit length of B to form a plurality of promoted multibit portions, such that said promoted multibit portions may be abutted to form a promoted data word ~~P~~; and

(iv) performing a plurality of independent arithmetic operations using as input operands respective bit position portions of bit length B from both said promoted data word ~~P~~ and said second, different input data word ~~Rn~~ to form a result data word ~~Rd~~.

15. (Original) A computer program product comprising a computer program for controlling a computer to perform a method as claimed in claim 14.